

ONLINE HIGH LEVEL SYNTHESIS

Chen Yingxi

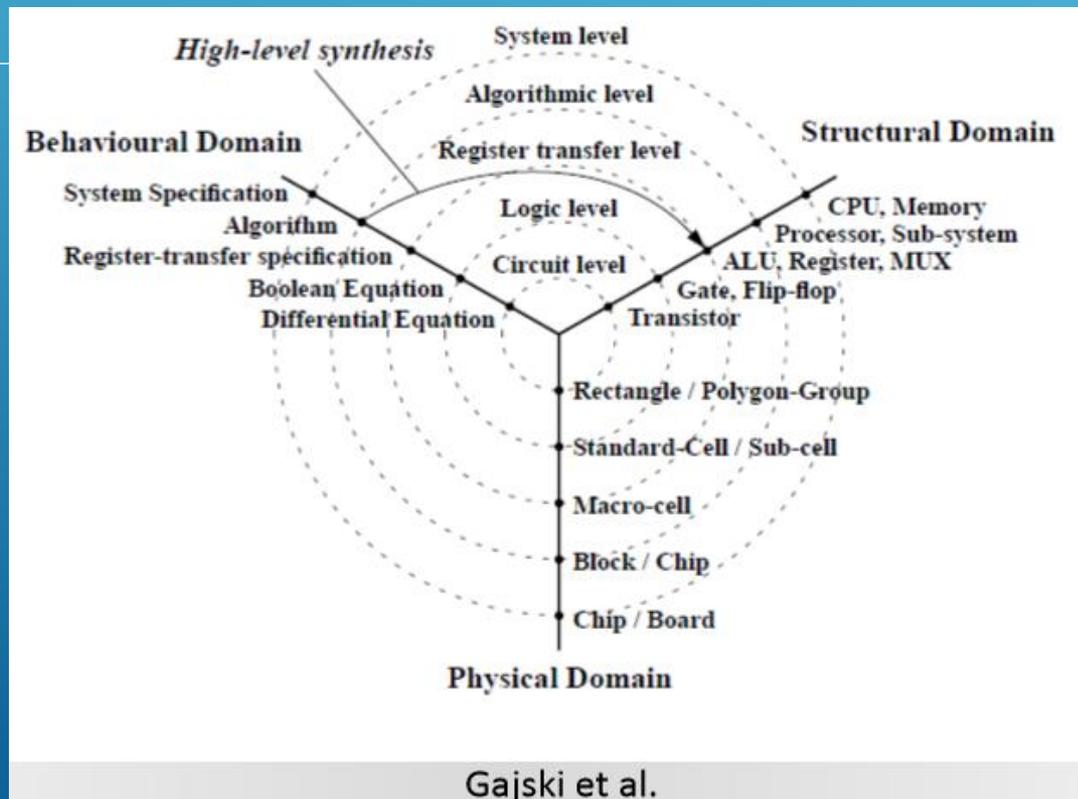
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A series of several parallel white lines of varying thicknesses, slanted diagonally from the bottom-left towards the top-right, located in the lower right quadrant of the slide.

WHAT IS HIGH LEVEL SYNTHESIS

▶ Definition:

- ▶ “Automatic conversion of behavioral, untimed descriptions into hardware that implements that behavior” .
- ▶ Transfer ANSI-C description to VHDL (or Verilog) Description



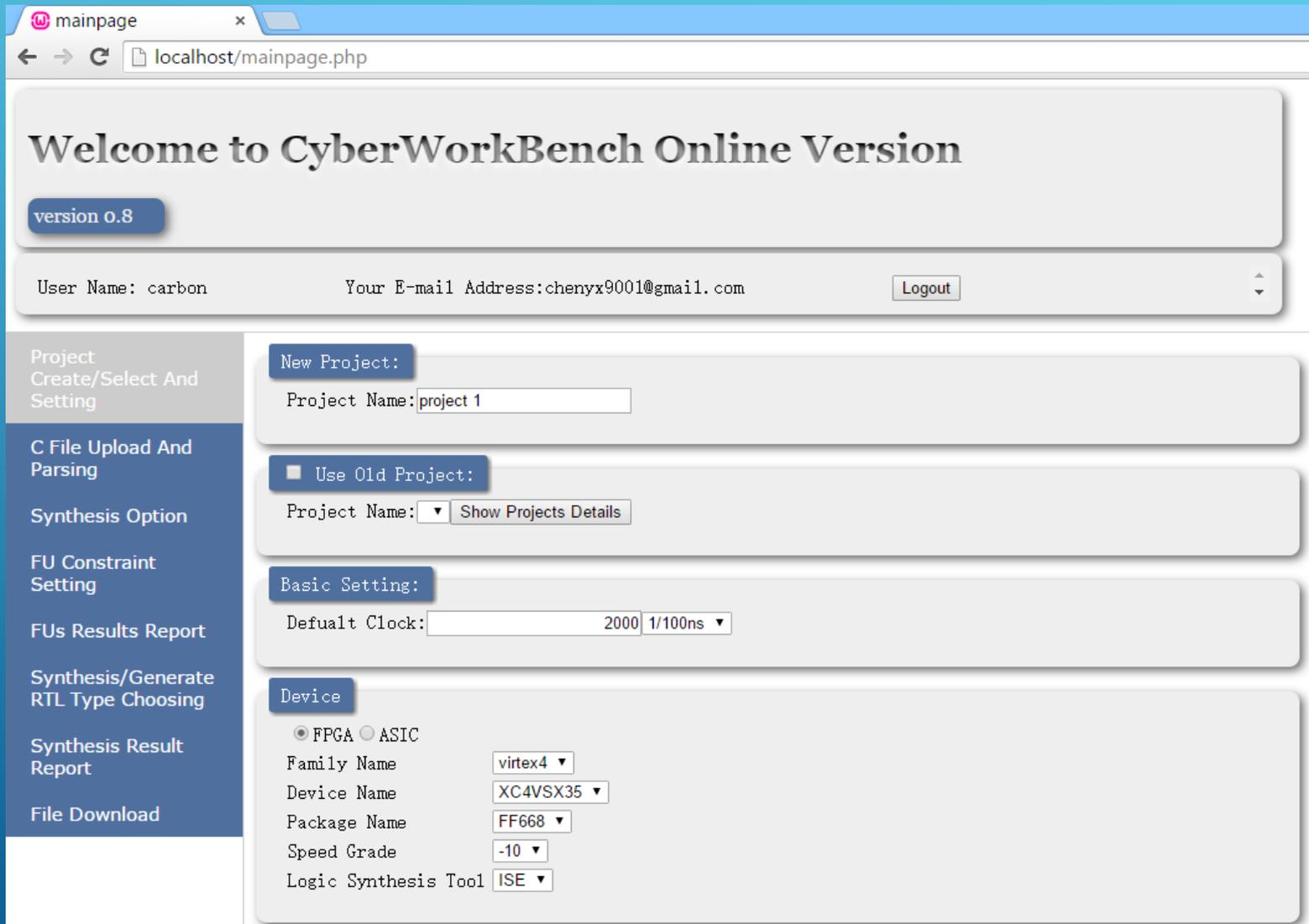
WHY ONLINE?

- ▶ Web Service
 - ▶ self-describing software modules that can be programmatically invoked over the Internet.
 - ▶ Advantage
 - ▶ Discoverable
 - ▶ Cost reduction
 - ▶ Better Security
 - ▶ Better Utilization
 - ▶ Ease HW and SW maintenance (Upgrade and failed)
 - ▶ Operation system independence
- 

WHAT CAN IT DO?

- ▶ User management
 - ▶ File Management
 - ▶ File Upload and download
 - ▶ Project Zip
 - ▶ Graphical User Interface
 - ▶ Function Constraint file generation
 - ▶ High level Synthesis
 - ▶ Quality of Report
- 

BRIEF INTRODUCTION



mainpage x
localhost/mainpage.php

Welcome to CyberWorkBench Online Version

version 0.8

User Name: carbon Your E-mail Address: chenyx9001@gmail.com Logout

Project Create/Select And Setting

New Project:
Project Name: project 1

Use Old Project:
Project Name: Show Projects Details

Basic Setting:
Default Clock: 2000 1/100ns

Device
 FPGA ASIC
Family Name: virtex4
Device Name: XC4VSX35
Package Name: FF668
Speed Grade: -10
Logic Synthesis Tool: ISE

BRIEF INTRODUCTION

The screenshot displays the CyberWorkBench Online Version web interface. The browser address bar shows the URL `localhost/mainpage.php`. The main heading is "Welcome to CyberWorkBench Online Version" with a sub-heading "version 0.8". The user information section shows "User Name: carbon" and "Your E-mail Address: chenyx9001@gmail.com" with a "Logout" button.

The left sidebar contains a navigation menu with the following items:

- Project Create/Select And Setting
- C File Upload And Parsing
- Synthesis Option
- FU Constraint Setting
- FUs Results Report
- Synthesis/Generate RTL Type Choosing
- Synthesis Result Report
- File Download

The main content area is divided into several sections:

- Basic Setting**
 - Mode
 - Clock/Reset
 - Specify Clock_constraint
- Library**
 - FU Libraries
 - Memory Libraries
 - Other Libraries
- Synthesize Planning**
 - Macro
 - Error
- Detail Setting**
 - Circuit Specification1
 - Language-Level Optimization
 - Other Optimization
 - Scheduling

The right-hand side of the main content area contains three configuration panels:

- Scheduling Mode**
 - Manual scheduling
 - Automatic scheduling
 - Automatic pipeline Scheduling (Data Initiation Interval=1 cycle)
- Synthesize as a lower hierarchical module**
 - Synthesize as a lower hierarchical module
- lower hierarchical module**
 - default value for input signals of lower hierarchical modules Don't care 0

The status bar at the bottom of the page shows the URL `localhost/synthesisoption.php`.

BRIEF INTRODUCTION

The screenshot shows a web browser window with the URL localhost/mainpage.php. The page title is "Welcome to CyberWorkBench Online Version" and the version is 0.8. The user is logged in as "carbon" with the email address "chenyx9001@gmail.com". The interface is divided into a left sidebar and a main content area. The sidebar contains navigation links for Project, C File Upload And Parsing, Synthesis Option, FU Constraint Setting, FUs Results Report, Synthesis/Generate RTL Type Choosing, Synthesis Result Report, and File Download. The main content area is titled "Select the type of description you want to synthesis your file to:" and contains several sections for file generation and command selection.

mainpage x
localhost/mainpage.php

Welcome to CyberWorkBench Online Version

version 0.8

User Name: carbon Your E-mail Address:chenyx9001@gmail.com Logout

Project
Create/Select And Setting

C File Upload And Parsing

Synthesis Option

FU Constraint Setting

FUs Results Report

Synthesis/Generate RTL Type Choosing

Synthesis Result Report

File Download

Select the type of description you want to synthesis your file to:

FCNT File Generation

Generate Generate Command for Function unit constraint file(.FCNT)

GenerateFCNT Generate FCNT file

Selection for VHDL or Verilog Generation Command

Select Verilog Command Select Verilog Description

Select VHDL Command Select VHDL Description

VHDL and Verilog File Generation

Generate result Generate Verilog file selected above

Generate result Generate VHDL file selected above

Reset

Reset FU constraint reset library

BRIEF INTRODUCTION

mainpage x
localhost/mainpage.php

Welcome to CyberWorkBench Online Version

version 0.8

User Name: carbon Your E-mail Address: chenyx9001@gmail.com Logout

- Project Create/Select And Setting
- C File Upload And Parsing
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- Synthesis Result Report
- File Download

Project Status

relative project directory :
/.QOR.HTML
Project name :
top module file name :

report area

cannot find the QOR report
Probably due to fail of the synthesis, please try to synthesis again

no error report exist yet, please check the parsing procedure with content below:

BRIEF INTRODUCTION

The screenshot shows a web browser window with the address bar displaying 'localhost/mainpage.php'. The main content area features a large heading 'Welcome to CyberWorkBench Online Version' and a sub-heading 'version 0.8'. Below this, the user's name 'carbon' and email address 'chenyx9001@gmail.com' are shown, along with a 'Logout' button. A left sidebar contains a menu with options: 'Project Create/Select And Setting', 'C File Upload And Parsing', 'Synthesis Option', 'FU Constraint Setting', 'FUs Results Report', 'Synthesis/Generate RTL Type Choosing', 'Synthesis Result Report', and 'File Download'. The main content area also includes a 'Project Status' section with the following information: 'Current User : carbon', 'Current Project :', and 'Current Top Module :'. Below this information are two buttons labeled 'zip' and 'download'.

mainpage x
localhost/mainpage.php

Welcome to CyberWorkBench Online Version

version 0.8

User Name: carbon Your E-mail Address:chenyx9001@gmail.com Logout

Project Create/Select And Setting

C File Upload And Parsing

Synthesis Option

FU Constraint Setting

FUs Results Report

Synthesis/Generate RTL Type Choosing

Synthesis Result Report

File Download

Project Status

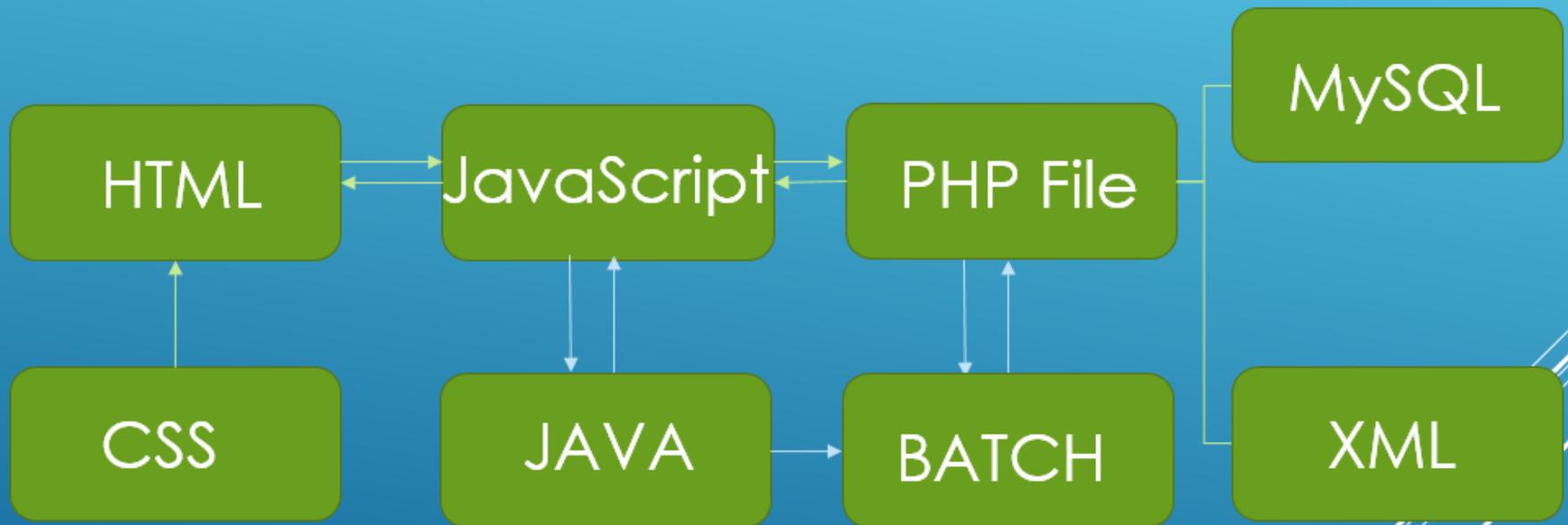
Current User :
carbon

Current Project :

Current Top Module :

zip download

WHAT TECHNIQUE IS USED?



WHAT TECHNIQUE IS USED?

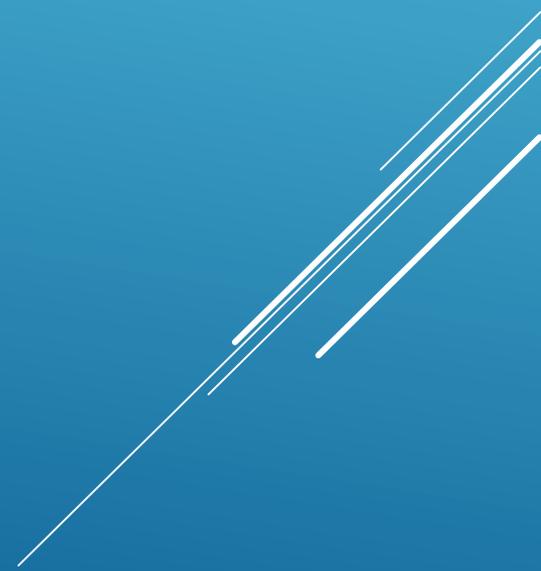
WAMP Platform

- ▶ Operation system -> W -> Windows
 - ▶ Server -> A -> Apache
 - ▶ Database -> M -> MySQL
 - ▶ Script Language -> P -> PHP
-
- ▶ Advantage:
 - ▶ 1. Free
 - ▶ 2. Open Source
 - ▶ 3. Easy to implement

WHAT TECHNIQUE IS USED?

- ▶ AJAX (Asynchronous JavaScript and XML)
 - ▶ Communicate between Browser and server
 - ▶ Javascript and JQuery
 - ▶ Dynamic Webpage response and animation
 - ▶ REST (Representational State Transfer)
 - ▶ Calling Java servlet
 - ▶ Java
 - ▶ Execute CyberworkBench, Create runtime environment
 - ▶ PHP
 - ▶ Main frame work for the server side structure
 - ▶ Response to most of the browser requests
 - ▶ XML (eXtensible Markup Language)
 - ▶ Store Function library, file management
 - ▶ MySQL
 - ▶ Store users' information
 - ▶ CSS
 - ▶ Interface beautify
- 

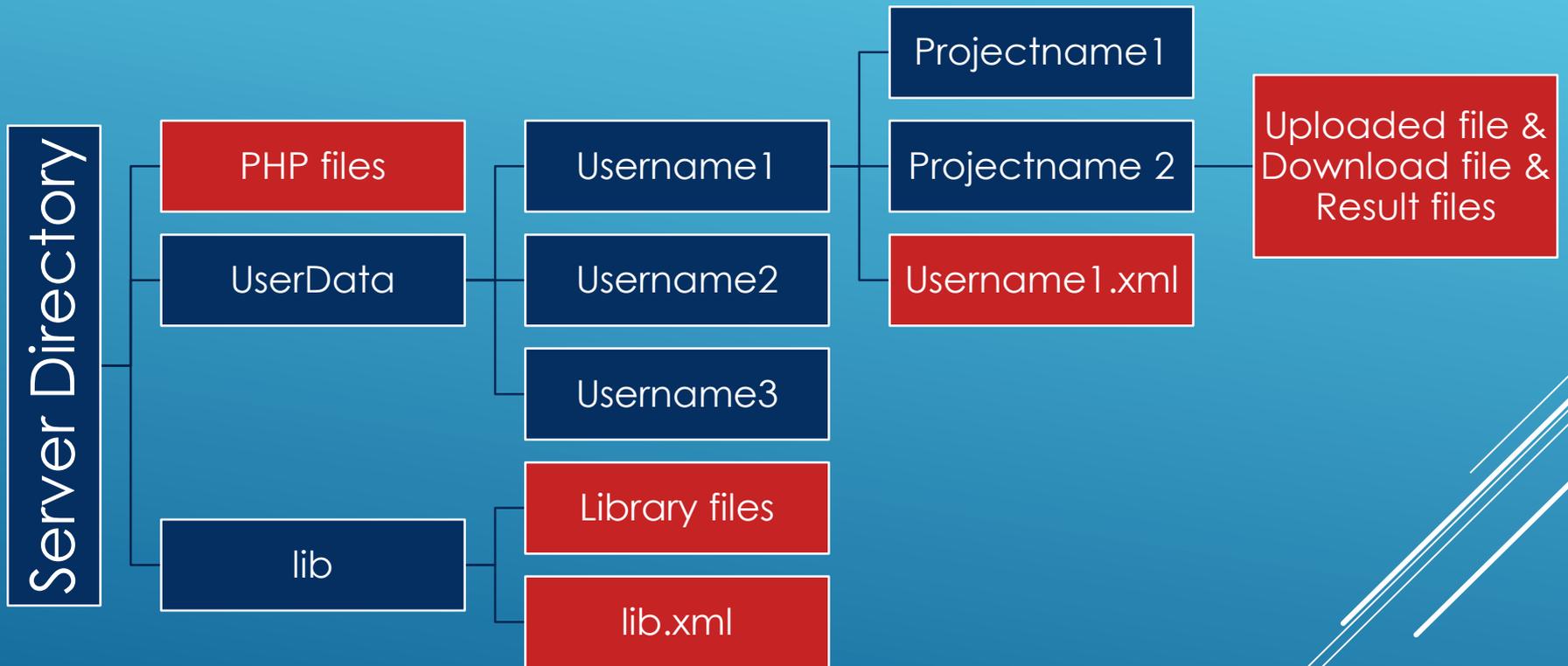
PROJECT CHARACTERISTIC

- ▶ Atomic transaction
 - ▶ Strict User Input checking
 - ▶ Flexible File Management system
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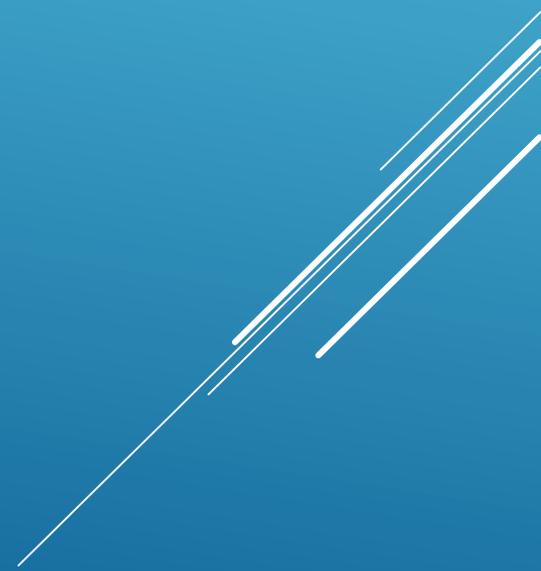
FLOW CHART



SERVER STRUCTURE



FAST DEMONSTRATION



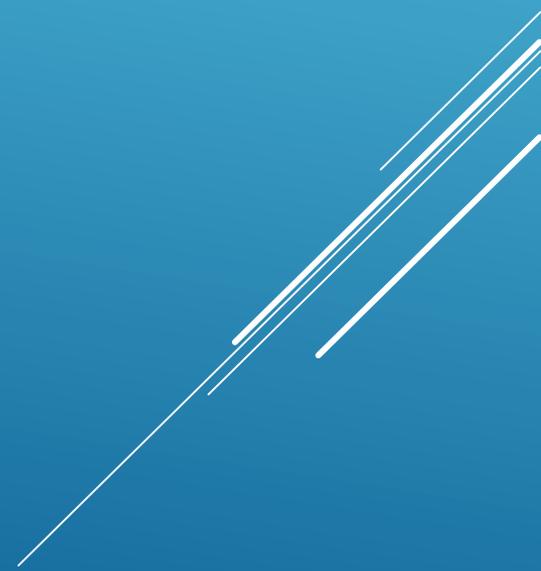
- ▶ Edit C code directly in browser
- ▶ Identification Code
- ▶ File upload checking
- ▶ Additional functions
- ▶ Multithreading
- ▶ Linux system runtime support

POSSIBLE FUTURE IMPROVEMENT



- ▶ In my opinion, this project can really spread out the idea of high level synthesis and reduce the time and cost to access such a service. In one word, the project is both practical and useful.

SUMMARY



Q & A

